AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Currently Amended) ~~An~~ A high speed adder ~~according to claim 1~~ in which provisional carries composed of a pair of signals that indicate a case where carry is produced from a low order bit and a case where no carry is produced therefrom are generated in advance and an actual carry is selected from the provisional carries in accordance with selection information from the low order bit, the high speed added comprising:

a carry transfer path; and

a plurality of converters, each of which converts the provisional carries into provisional sums composed of a pair of signals that indicate the case where the carry is produced from the low order bit and the case where no carry is produced therefrom, the converters being provided on a predetermined portion of the carry transfer path,

wherein, when the adder is a 2^N(N is an integer of 3 or more)-bit adder, the ~~carrier~~carry transfer path comprises (N+1) or less circuit stages,

wherein a first circuit stage receives two input data for each corresponding bit and an input carry signal from an outside, generates a bit sum of a least significant bit, outputs the bit sum to the outside, generates provisional ~~carriers~~carries corresponding to each of bits other than the least significant bit, and outputs the generated provisional ~~carriers~~carries to a following circuit stage,

wherein second to N-th circuit stages convert the provisional ~~carriers~~carries corresponding to higher $(2^{(N-1)}-1)$ bits other than a most significant bit, of the provisional ~~carriers~~carries into the provisional sums by at least one of the converters in course of transfer,

and generate actual ~~carriers~~carries from the provisional ~~carriers~~carries corresponding to lower $(2^{(N-1)}-1)$ bits other than the least significant bit, and

wherein a (N+1)-th circuit stage outputs data other than a bit sum of the least significant bit, of sum data of the two input data and an output carry signal to the outside.

3. (Original) An adder according to claim 2, wherein, when the input data is arranged in an order from the most significant bit to the least significant bit, at least one of the converters is located corresponding to a $(2^{(N-M-1)}+1)$-th bit to a $2^{(N-M)}$-th bit from the most significant bit of the input data in a (N-M+1)-th circuit stage which is specified by an integer M that satisfies $1 \leq M < N$.

4. (Currently Amended) An adder according to claim 2, wherein the first circuit stage comprises:

(2^N-1) conditional cells, each of which receives corresponding bits of the two input data to perform an exclusive OR operation, generates the provisional ~~carriers~~carries composed of the pair of signals that indicate the case where the carry is produced from the low order bit and the case where no carry is produced therefrom, and outputs the generated provisional ~~carriers~~carries, the conditional cells being provided corresponding to a most significant bit of 2^N bits to a bit higher than the least significant bit thereof by one; and

a full adder that receives the least significant bits of the two input data and the output carry signal and generates an exclusive OR signal and a carry signal.

5. (Original) An adder according to claim 4, wherein each of the conditional cells comprises:

a first gate that receives two input bits and performs an AND operation on the two input bits to output a first signal;

a second gate that receives the two input bits and performs an OR operation on the two input bits to output a second signal;

a third gate that receives the first signal outputted from the first gate and inverts the received first signal to output a third signal; and

a fourth gate that receives the second signal outputted from the second gate and the third signal outputted from the third gate and performs the AND operation on the second signal and the third signal to output a fourth signal,

wherein the first signal outputted from the first gate is given as a first carry signal which is the carry signal in the case where no carry is produced from the low order bit,

wherein the second signal outputted from the second gate is given as a second carry signal which is the carry signal in the case where the carry is produced from the low order bit, and

wherein the fourth signal outputted from the fourth gate is a result of the exclusive OR operation performed on the two input bits.

6. (Currently Amended) An adder according to claim 4, wherein, of the circuit stages, when the (N-M+1)-th circuit stage which is specified by the integer M that satisfies $1 \leq M < N$ is divided in a virtual form into 2^M sub-circuits corresponding to every $2^{(N-M)}$ bits of the input data,

the (N-M+1)-th circuit stage comprises:

$2^{(N-M-1)}$ multiplexers, each of which receives a pair of signals which are outputs of one of the conditional cell and the carry selector which are provided for a corresponding bit in a

preceding circuit stage; receives a signal outputted from one of the full adder and the multiplexer which are provided for a bit in a circuit stage preceding by one stage, and which corresponds to a $(2^{(N-M-1)}+1)$-th bit from a top in a first sub-arithmetic circuit; selects an actual carry signal in accordance with the received signal; and outputs the actual carry signal, the multiplexers being provided corresponding to higher $2^{(N-M-1)}$ bits of the first sub-arithmetic circuit which include an input from a bit corresponding to a $2^{(N-M)}$-th bit from the least significant bit in a high order direction;

$(2^{(N-1)} - 2^{(N-M-1)})$ carry selectors, each of which receives a pair of signals which are outputs of one of the conditional cell, the carry selector, and the converter, which are provided for the corresponding bit in the preceding circuit stage; receives a pair of selection signals which are outputs of one of the conditional cell and the carry selector which are provided for a bit in the circuit stage preceding by one stage, and which corresponds to the $(2^{(N-M-1)}+1)$-th bit from the top in a sub-circuit; selects a pair of signals indicating the provisional ~~carriers~~ carries or the provisional sums in the following circuit stage in accordance with the selection signals; and outputs the selected pair of signals, the carry selectors being provided corresponding to the higher $2^{(N-M-1)}$ bits in the sub-circuit which is included in a second sub-arithmetic circuit composed of a sub-circuit that receives a carry signal corresponding to the most significant bit or a third sub-arithmetic circuit composed of second to $(2^{M}-1)$-th sub-circuits from the second sub-arithmetic circuit in the low order direction; and

$2^{(N-M-1)}$ converters, each of which receives a pair of signals which are outputs of one of the conditional cell and the carry selector which are provided for the corresponding bit in the preceding circuit stage and indicate the provisional ~~carriers~~carries, and an exclusive OR signal outputted from the conditional cell corresponding to a bit higher by one bit in the first circuit

stage; converts the received pair of signals into a pair of signals indicating the provisional sums; and outputs the pair of signals indicating the provisional sums, the converters being provided corresponding to lower $2^{(N-M-1)}$ bits in the second sub-arithmetic circuit.

7. (Original) An adder according to claim 6, wherein each of the conditional cells comprises:

a first gate that receives two input bits and performs an AND operation on the two input bits to output a first signal;

a second gate that receives the two input bits and performs an OR operation on the two input bits to output a second signal;

a third gate that receives the first signal outputted from the first gate and inverts the received first signal to output a third signal; and

a fourth gate that receives the second signal outputted from the second gate and the third signal outputted from the third gate and performs an AND operation on the second signal and the third signal to output a fourth signal,

wherein the first signal outputted from the first gate is given as a first carry signal which is the carry signal in the case where no carry is produced from the low order bit,

wherein the second signal outputted from the second gate is given as a second carry signal which is the carry signal in the case where the carry is produced from the low order bit, and

wherein the fourth signal outputted from the fourth gate is a result of the exclusive OR operation performed on the two input bits.

8. (Currently Amended) An adder according to claim 6, whercin each of the converters comprises:

a first exclusive OR circuit that receives one of the pair of signals indicating the provisional ~~carriers~~ carries and the exclusive OR signal outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage and outputs one of the pair of signals indicating the provisional sums; and

a second exclusive OR circuit that receives the other of the pair of signals indicating the provisional ~~carriers~~ carries and the exclusive OR signal, and outputs the other of the pair of signals indicating the provisional sums.

9. (Original) An adder according to claim 6, wherein each of the carry selectors comprises:

a first multiplexer that receives a pair of input signals indicating the provisional ~~carriers~~carries, selects one of the pair of input signals in accordance with one of the pair of selection signals, and outputs the selected one as one of a pair of output signals; and

a second multiplexer that receives the pair of input signals, selects one of the pair of input signals in accordance with the other of the pair of selection signals, and outputs the selected one as the other of the pair of output signals.

10. (Original) An adder according to claim 6, wherein the (N+1)-th circuit stage comprises:

a multiplexer that receives a pair of signals outputted from a highest order carry selector provided corresponding to the most significant bit of the input data in the N-th circuit stage, selects an output carry signal in accordance with the selection signal outputted the multiplexer

corresponding to a $(2^{(N-1)}+1)$-th bit from the most significant bit of the input data in the low order direction in the N-th circuit stage, and outputs the output carry signal;

$(2^{(N-1)}-1)$ multiplexers, each of which receives the pair of signals outputted from one of the carry selector and the converter which are provided for a corresponding bit in the N-th circuit stage, selects a signal corresponding to an actual bit sum of a bit higher by one bit in accordance with the selection signal outputted from the multiplexer corresponding to the $(2^{(N-1)}+1)$-th bit from the most significant bit of the input data in the low order direction in the N-th circuit stage, and outputs the signal corresponding to an actual bit sum of a bit higher by one bit, the multiplexers being provided corresponding to a second bit to a $2^{(N-1)}$-th bit from the most significant bit of the input data in the low order direction; and

$2^{(N-1)}$ exclusive OR circuits, each of which receives the actual carry signal outputted from one of the full adder and the multiplexer which are provided for the corresponding bit in a preceding circuit stage and the exclusive OR signal outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage, and outputs a signal corresponding to an actual bit sum of a bit higher by one bit, the exclusive OR circuits being provided corresponding to a $(2^{(N-1)}+1)$-th bit to a 2^{N}-th bit from the most significant bit of the input data in the low order direction.

11. (Original) An adder according to claim 10, wherein each of the conditional cells comprises:

a first gate that receives two input bits and performs an AND operation on the two input bits to output a first signal;

a second gate that receives the two input bits and performs an OR operation on the two input bits to output a second signal;

a third gate that receives the first signal outputted from the first gate and inverts the received first signal to output a third signal; and

a fourth gate that receives the second signal outputted from the second gate and the third signal outputted from the third gate and performs the AND operation on the second signal and the third signal to output a fourth signal,

wherein the first signal outputted from the first gate is given as a first carry signal which is the carry signal in the case where no carry is produced from the low order bit,

wherein the second signal outputted from the second gate is given as a second carry signal which is the carry signal in the case where the carry is produced from the low order bit, and

wherein the fourth signal outputted from the fourth gate is a result of the exclusive OR operation on the two input bits.

12. (Currently Amended) An adder according to claim 10, wherein each of the converters comprises:

a first exclusive OR circuit that receives one of the pair of signals indicating the provisional ~~carriers~~ carries and the exclusive OR signal outputted from the conditional cell corresponding to the bit higher by one bit in the first circuit stage, and outputs one of the pair of signals indicating the provisional sums; and

a second exclusive OR circuit that receives the other of the pair of signals indicating the provisional ~~carriers~~carries and the exclusive OR signal, and outputs the other of the pair of signals indicating the provisional sums.

13. (Original) An adder according to claim 10, wherein each of the carry selectors comprises:

a first multiplexer that receives a pair of input signals indicating the provisional ~~carriers~~carries, selects one of the pair of input signals in accordance with one of the pair of selection signals, and outputs the selected one as one of a pair of output signals; and

a second multiplexer that receives the pair of input signals, selects one of the pair of input signals in accordance with the other of the pair of selection signals, and outputs the selected one as the other of the pair of output signals.

14. (New) An adder calculating a sum of numbers A and B, said number A being expressed by at least five binary bits A_1, A_2, A_3, A_4, and A_5, said A_2 being less significant than said A_1, said A_3 being less significant than said A_2, said A_4 being less significant than said A_3, said A_5 being less significant than said A_4, said number B being expressed by at least five binary bits B_1, B_2, B_3, B_4, and B_5, said B_2 being less significant than said B_1, said B_3 being less significant than said B_2, said B_4 being less significant than said B_3, said B_5 being less significant than said B_4, said adder comprising:

a first conditional cell receiving said binary bits A_1 and B_1 and outputting a pair of first provisional carries and a first exclusive OR of said binary bits A_1 and B_1, one of said first provisional carries indicating a carry generated by a sum of said binary bits A_1 and B_1 providing that a sum of said binary bits A_2 and B_2 generates a carry, another of said first provisional carries indicating a carry generated by said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_2 and B_2 generates no carry;

a second conditional cell receiving said binary bits A_2 and B_2 and outputting a pair of second provisional carries and a second exclusive OR of said binary bits A_2 and B_2, one of said

second provisional carries indicating a carry generated by said sum of said binary bits A_2 and B_2 providing that a sum of said binary bits A_3 and B_3 generates a carry, another of said second provisional carries indicating a carry generated by said sum of said binary bits A_2 and B_2 providing that said sum of said binary bits A_3 and B_3 generates no carry;

a third conditional cell receiving said binary bits A_3 and B_3 and outputting a pair of third provisional carries and a third exclusive OR of said binary bits A_3 and B_3, one of said third provisional carries indicating a carry generated by said sum of said binary bits A_3 and B_3 providing that a sum of said binary bits A_4 and B_4 generates a carry, another of said third provisional carries indicating a carry generated by said sum of said binary bits A_3 and said B_3 providing that said sum of said binary bits A_4 and B_4 generates no carry;

a fourth conditional cell receiving said binary bits A_4 and B_4 and outputting a pair of fourth provisional carries and a fourth exclusive OR of said binary bits A_4 and B_4, one of said fourth provisional carries indicating a carry generated by said sum of said binary bits A_4 and B_4 providing that a sum of said binary bits A_5 and B_5 generates a carry, another of said fourth provisional carries indicating a carry generated by said sum of said binary bits A_4 and B_4 providing that said sum of said binary bits A_5 and B_5 generates no carry;

a first carry selector receiving said pair of first provisional carries and said pair of second provisional carries and outputting a pair of fifth provisional carries, one of said fifth provisional carries indicating a carry generated by said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_3 and B_3 generates a carry, another of said fifth provisional carries indicating a carry generated by said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_3 and B_3 generates no carry;

a second carry selector receiving said pair of third provisional carries and said pair of fourth provisional carries and outputting a pair of sixth provisional carries, one of said sixth provisional carries indicating a carry generated by said sum of said binary bits A_3 and B_3 providing that said sum of said A_5 and B_5 generates a carry, another of said sixth provisional carries indicating a carry generated by said sum of said binary bits A_3 and B_3 providing that said sum of said binary bits A_5 and B_5 generates no carry;

a first converter receiving said first exclusive OR and said pair of second provisional carries and outputting a pair of first provisional sums, one of said first provisional sums indicating said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_3 and B_3 generates a carry, another of said first provisional sums indicating said sum of said binary bits A_1 and B_1 providing said sum of said binary bits A_3 and B_3 generates no carry; and

a second converter receiving said second exclusive OR and said pair of said sixth provisional carries and outputting a pair of second provisional sums, one of said second provisional sums indicating said sum of said binary bits A_2 and B_2 providing that said sum of said binary bits A_5 and B_5 generates a carry, another of said second provisional sums indicating said sum of said binary bits A_2 and B_2 providing that said sum of said binary bits A_5 and B_5 generates no carry.

15. (New) The adder according to claim 14, further comprising:

a third carry selector receiving said first provisional sums and said sixth provisional carries and outputting a pair of third provisional sums, one of said third provisional sums indicating said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_5

and B_5 generates a carry, another of said third provisional sums indicating said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_5 and B_5 generates no carry.

16. (New) The adder according to claim 15, further comprising:

a fourth carry selector receiving said pair of fifth provisional carries and said pair of sixth provisional carries and outputting a pair of seventh provisional carries, one of said seventh provisional carries indicating a carry generated by said sum of said binary bits A_1 and B_1 providing that said sum of said A_5 and B_5 generates a carry, another of said seventh provisional carries indicating a carry generated by said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_5 and B_5 generates no carry.

17. (New) An adder calculating a sum of numbers A and B,

said number A being expressed by at least four binary bits A_1, A_2, A_3, and A_4, said A_2 being less significant than said A_1, said A_3 being less significant than said A_2, said A_4 being less significant than said A_3, said number B being expressed by at least four binary bits B_1, B_2, B_3, and B_4, said B_2 being less significant than said B_1, said B_3 being less significant than said B_2, said B_4 being less significant than said B_3, said adder comprising:

a first conditional cell receiving said binary bits A_1 and B_1 and outputting a pair of first provisional carries and a first exclusive OR of said binary bits A_1 and B_1, one of said first provisional carries indicating a carry generated by a sum of said binary bits A_1 and B_1 providing that a sum of said binary bits A_2 and B_2 generates a carry, another of said first provisional carries indicating a carry generated by said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_2 and B_2 generates no carry;

a second conditional cell receiving said binary bits A_2 and B_2 and outputting a pair of second provisional carries and a second exclusive OR of said binary bits A_2 and B_2, one of said second provisional carries indicating a carry generated by said sum of said binary bits A_2 and B_2 providing that a sum of said binary bits A_3 and B_3 generates a carry, another of said second provisional carries indicating a carry generated by said sum of said binary bits A_2 and B_2 providing that said sum of said binary bits A_3 and B_3 generates no carry;

a third conditional cell receiving said binary bits A_3 and B_3 and outputting a pair of third provisional carries and a third exclusive OR of said binary bits A_3 and B_3, one of said third provisional carries indicating a carry generated by said sum of said binary bits A_3 and B_3 providing that a sum of said binary bits A_4 and B_4 generates a carry, another of said third provisional carries indicating a carry generated by said sum of said binary bits A_3 and B_3 providing that said sum of said binary bits A_4 and B_4 generates no carry;

a first carry selector receiving said pair of second provisional carries and said pair of third provisional carries and outputting a pair of fourth provisional carries, one of said fourth provisional carries indicating a carry generated by said sum of said binary bits A_2 and B_2 providing that said sum of said binary bits A_4 and B_4 generates a carry, another of said fourth provisional carries indicating a carry generated by said sum of said binary bits A_2 and B_2 providing that said sum of said binary bits A_4 and B_4 generates no carry; and

a first converter receiving said first exclusive OR and said pair of fourth provisional carries and outputting a pair of first provisional sums, one of said first provisional sums indicating said sum of said binary bits A_1 and B_1 providing that said sum of said binary bits A_4 and B_4 generates a carry, another of said first provisional sums indicating said sum of said binary bits A_1 and B_1 providing said sum of said binary bits A_4 and B_4 generates no carry.